| Notice of Allowability | Application No. | Applicant(s) | |
|---|---|---|---|
| | 09/726,188 | PARVIAINEN, JARI A. | |
| | Examiner | Art Unit | |
| | Chat C. Do | 2193 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--*

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *01/24/05*.

2. ☒ The allowed claim(s) is/are *1-7,10-16,19-21,23 and 24*.

3. ☒ The drawings filed on *29 November 2000* are accepted by the Examiner.

4. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☐ All b) ☐ Some* c) ☐ None of the:
      1. ☐ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
**THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.**

5. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

6. ☐ CORRECTED DRAWINGS ( as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review ( PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   **Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).**

7. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

**Attachment(s)**

1. ☐ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☐ Information Disclosure Statements (PTO-1449 or PTO/SB/08), Paper No./Mail Date _____
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application (PTO-152)
6. ☒ Interview Summary (PTO-413), Paper No./Mail Date *attached* .
7. ☒ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

## EXAMINER'S AMENDMENT

1. An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

Authorization for this examiner's amendment was given in a telephone interview with Mr. Robert J. Mauri on 05/24/2005.

The application has been amended following independent claims for further defining the claimed invention:

Claim 1. (Currently Amended) A data processor, comprising a multiplier block having a multiplier front end for generating partial products from input operands, and a plurality of arithmetic logic units (ALUs) having inputs switchably coupled, in a first mode of operation, to first data sources comprised of outputs of said multiplier front end for adding together partial products received therefrom to arrive at a multiplication result, said inputs of said plurality of ALUS being switchably coupled, in a second mode of operation, to second data sources for performing at least one of arithmetic and logical operations on data received from said second data sources, wherein said plurality of ALUS, when in the second mode of operation, operate in parallel with one another on data received from said second data sources, and wherein said data processor forms a part of a wireless terminal.

Claim 10. (Currently Amended) A method of operating a data processor, comprising: providing a multiplier block having a multiplier front end for generating partial products from input operands, and providing said multiplier block with a plurality of arithmetic logic units (ALUs), wherein in a first mode of operation, said plurality of ALUS have inputs switchably coupled to first data sources comprised of outputs of said multiplier front end for adding together partial products received therefrom to arrive at a multiplication result; and in a second mode of operation, said inputs of said plurality of ALUS are switchably coupled to second data sources for performing at least one of arithmetic and logical operations on data received from said second data sources, wherein said plurality of ALUS, when in the second mode of operation, operate in parallel with one another on data received from said second data sources, and wherein said data processor forms a part of a wireless terminal.

Claim 21. (Currently Amended) A digital signal processor (DSP), comprising a DSP core having a register file, at least one arithmetic logical unit (ALU), and at least one multiplier block comprised of a multiplier front end for generating partial products from input operands, said multiplier block further comprising circuitry for adding together said partial products, said circuitry comprising a plurality of ALUS having inputs that are programmably coupled, in a first mode of operation, to first data sources comprised of outputs of said multiplier front end for adding together partial products received therefrom to arrive at a multiplication result, said inputs of said plurality of ALUs being programmably coupled, in a second mode of operation, to second data sources for selectively operating together in parallel for performing at least one of

arithmetic and logical operations on data received from said second data sources, wherein said partial products have a width of n-bits, and where a width of individual ones of said plurality of ALUS is one of n-bits or less than n-bits, wherein said DSP forms a part of a wireless terminal.

## REASONS FOR ALLOWANCE

2. Claims 1-7, 10-16, 19-21, and 23-24 are allowed.

3. Claims 8-9, 17-18, and 22 are cancelled.

4. The following is an examiner's statement of reasons for allowance:

The prior art of records fails to disclose or render an obviousness of a data processor comprising a multiplier block having a multiplier front end for generating partial products; and a plurality of arithmetic logic units having inputs switchably coupled to add all partial products to form a multiplication result in a first mode and to perform at least one of arithmetic and logical operations on data received from second data source in a second mode and operate in parallel with one another on data received from said second data sources wherein the data processor is part of a wireless terminal as cited in independent claims 1, 10, and 21.

The closest found prior art is Abdallah et al. (U.S. 6,377,970). Abdallah et al. disclose a method and apparatus for computing a sum of packed data elements using SIMD multiply circuitry including a multiplier block for generating a product in a first

mode and generating a sum in a second mode. However, Abdallah et al. fail to disclose, show, or teach structurally the performance at least one of arithmetic and logical operations on data received from second data source in second mode and the apparatus is part of a wireless terminal as cited above.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Chat C. Do whose telephone number is (571) 272-3721. The examiner can normally be reached on 7:00AM to 5:00PM M-Th.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chaki Kakali can be reached on (571) 272-3719. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Chat C Do
Examiner
Art Unit 2193

May 24, 2005

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